ABSTRACT OF THE DISCLOSURE

A processor supports multiple operand sizes (e.g. 8, 16, 32, and 64 bit operand sizes, in one embodiment). Additionally, the processor determines how to update a destination register when an operand size less than the largest operand size is used. In one embodiment, the processor determines whether or not to zero extend the result responsive to the operand size used. In one particular embodiment, the processor zero extends 32 bit operands and does not zero extend 8 or 16 bit operands. Furthermore, the processor may preserve the value in at least part of the remaining portion of the register when 8 or 16 bit operand sizes are used.